UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,355	09/11/2003	Mark F. Kelcourse	17988	7884

26794 7590 06/05/2007
TYCO TECHNOLOGY RESOURCES
4550 NEW LINDEN HILL ROAD, SUITE 140
WILMINGTON, DE 19808-2952

EXAMINER	
GUZMAN, APRIL S	
ART UNIT	PAPER NUMBER
2618	
MAIL DATE	DELIVERY MODE
06/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/660,355	KELCOURSE, MARK F.	
	Examiner	Art Unit	
	April S. Guzman	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09/11/03,11/24/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *09/11/03,11/04/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statements submitted on 09/11/2003 and 11/04/2004 have been considered by the Examiner and made of record in the application file.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Gerlach et al. (U.S. Patent # 6,518,855)** in view of **Yamamoto et al. (U.S. Patent # 6,066,993)**.

Consider **claim 1**, Gerlach et al. teach a single-die integrated circuit for switching among a plurality of transmission ports and a plurality of receiver ports (Abstract, column 1 lines 63-67, column 2 lines 4-6, and column 3 lines 27-36), comprising:

a transmitter switching section having a plurality of transmission ports, operable to switch a selected one of the plurality of transmission ports to a transmission node (column 2 lines 20-32, column 2 lines 41-54, and column 3 lines 18-63); and

a receiver switching section having a plurality of receiver ports, operable to switch a selected one of the plurality of receiver ports to the transmission node (column 2 lines 20-32, column 2 lines 41-54, and column 3 lines 18-63).

However, Gerlach et al. fail to teach a transmitter switching section having a plurality of transmission ports, transmitter control circuitry operable to switch a selected one of the plurality of transmission ports to a transmission node; and a receiver switching section having a plurality of receiver ports, receiver control circuitry operable to switch a selected one of the plurality of receiver ports to the transmission node.

In the related art, Yamamoto et al. teach a transmitter switching section having a plurality of transmission ports, transmitter control circuitry operable to switch a selected one of the plurality of transmission ports to a transmission node; and a receiver switching section having a plurality of receiver ports, receiver control circuitry operable to switch a selected one of the plurality of receiver ports to the transmission node (column 2 lines 63-67, column 3 lines 1-13, column 5 lines 13-22, column 5 lines 57-67, and column 6 lines 10-22).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Yamamoto et al. into the teachings of Gerlach et al. for the purpose of allowing the chip size to be remarkably reduced in the chip and reducing the insertion loss during transmission of the circuit with the impedance matching of the antenna with the receiver to be more easily achieved.

Consider **claim 2, as applied to claim 1 above**, Gerlach et al. as modified by Yamamoto et al. further teach wherein the receiver switching section includes at least two cascaded stages, a first cascaded stage controllable to switch the transmission node to a receiver node, a second cascaded stage controllable to switch the receiver node to a selected one of the plurality of receiver ports (Yamamoto et al. – column 10 lines 25-67, and column 11 lines 1-2).

Consider **claim 3, as applied to claim 1 above**, Gerlach et al. as modified by Yamamoto et al. further teach further comprising an antenna port coupled to the transmission node (Gerlach et al. – column 1 lines 41-47, and column 3 lines 18-26).

Consider **claim 4, as applied to claim 1 above**, Gerlach et al. as modified by Yamamoto et al. further teach wherein, for each transmission port, the transmitter switching section includes a series field effect transistor (FET) switching topology operable to couple the last said transmission port to the transmission node (Gerlach et al. – column 3 lines 37-45; and Yamamoto et al. – column 5 lines 57-67, column 6 lines 1-9, and column 11 lines 3-61).

Consider **claim 5, as applied to claim 4 above**, Gerlach et al. as modified by Yamamoto et al. further teach wherein each series FET switching topology comprises a plurality of FETs having current paths coupled in series with each other (Gerlach et al. – column 3 lines 37-45; and Yamamoto et al. – column 5 lines 57-67, column 6 lines 1-9, and column 11 lines 3-61).

Consider **claim 6, as applied to claim 4 above**, Gerlach et al. as modified by Yamamoto et al. further teach wherein at least one of the FET switching topologies includes at least one FET having a plurality of contiguous source regions interdigitated with a plurality of contiguous drain regions, a sinuous gate formed to wind between the source regions and the drain regions (Yamamoto et al. – column 5 lines 57-67, column 6 lines 1-9, and column 11 lines 3-61).

Consider **claim 7**, Gerlach et al. a single-die multiband switch for wireless communication (Abstract, column 1 lines 63-67, column 2 lines 4-6, column 2 lines 20-40, and column 3 lines 27-36), comprising:

an antenna port (column 3 lines 18-26);

a plurality of transmitter ports (column 3 lines 18-26); and

a plurality of receiver ports (column 3 lines 18-26).

However, Gerlach et al. fail to teach a switching topology operable to switch the last said transmitter port to the antenna port and a switching topology operable to switch the last said receiver port to the antenna port.

In the related art, Yamamoto et al. teach a switching topology operable to switch the last said transmitter port to the antenna port and a switching topology operable to switch the last said receiver port to the antenna port (column 5 lines 13-22, column 5 lines 57-67, and column 6 lines 10-22).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Yamamoto et al. into the teachings of Gerlach et al. for the purpose of allowing the chip size to be remarkably reduced in the chip and reducing the insertion loss during transmission of the circuit with the impedance matching of the antenna with the receiver to be more easily achieved.

Consider **claim 8, as applied to claim 7 above**, Gerlach et al. as modified by Yamamoto et al. further teach wherein at least one of the switching topologies comprises a plurality of series-connected field effect transistors, a control signal for said at least one switching topology controlling said at least one switching topology to selectively connect or isolate a respective

transmitter or receiver port from the antenna port (Gerlach et al. – column 3 lines 37-63; Yamamoto et al. – column 5 lines 57-67, and column 6 lines 10-22).

Consider **claim 9, as applied to claim 7 above**, Gerlach et al. as modified by Yamamoto et al. further teach wherein at least one of the switching topologies comprises at least one interdigitated field effect transistor having a plurality of elongated contiguous drain regions, a plurality of elongated contiguous source regions interdigitated with the drain regions, an elongated sinuous channel region spacing apart the drain regions from the source regions, and a gate overlying the channel region to switch the interdigitated field effect transistor between an ON and an OFF state (Gerlach et al. – column 3 lines 37-63; Yamamoto et al. – column 5 lines 57-67, column 6 lines 10-22, and column 6 lines 44-64).

Consider **claim 10, as applied to claim 7 above**, Gerlach et al. as modified by Yamamoto et al. further teach wherein the die has an area, the transmitter port switching topologies occupying an area on the die which is substantially larger than the receiver port switching topologies (Yamamoto et al. – column 11 lines 3-23, and column 11 lines 51-67).

Consider **claim 11, as applied to claim 7 above**, Gerlach et al. as modified by Yamamoto et al. further teach further including at least one multiple-stage switching topology, a first stage of the multiple-stage switching topology selectively connecting or isolating the antenna port from the multiple-stage switching topology, a last stage of the multiple-stage switching topology selectively connecting or isolating a plurality of other ports from the multiple-stage switching topology (Gerlach et al. – column 3 lines 18-63; Yamamoto et al. – column 5 lines 13-22, column 5 lines 57-67, and column 6 lines 1-22).

Consider **claim 12, as applied to claim 11 above**, Gerlach et al. as modified by Yamamoto et al. further teach wherein said other ports are receiver ports (Gerlach et al. – column 3 lines 18-26).

Consider **claim 13, as applied to claim 12 above**, Gerlach et al. as modified by Yamamoto et al. further teach wherein said last stage includes, for each receiver port, a signal path FET having a current path controllable to connect the receiver port to an intermediate node, said first stage operable to connect the intermediate node to the antenna port (Gerlach et al. – column 3 lines 18-63; Yamamoto et al. – column 5 lines 13-22, column 5 lines 57-67, and column 6 lines 1-22).

Consider **claim 14**, Gerlach et al. teach a single-die transmitter/receiver integrated switching circuit (Abstract, column 1 lines 63-67, column 2 lines 4-6, column 2 lines 20-40, and column 3 lines 27-36), comprising:

a plurality of transmitter ports (column 3 lines 18-26);

a plurality of receiver ports (column 3 lines 18-26);

at least one antenna port (column 3 lines 18-26);

a plurality of integrated circuit switching elements controllable to connect one of the transmitter ports or one of the receiver ports to the antenna port while isolating the remaining ones of the transmitter and receiver ports from the antenna port, at least one of the plurality of transmitter ports and the plurality of receiver ports being at least three in number (column 2 lines 20-32, column 2 lines 41-54, column 3 lines 18-26, and column 3 lines 37-63).

However, Gerlach et al. fail to teach at least some of the integrated circuit switching elements arranged in cascaded fashion in order to reduce signal insertion loss.

In the related art, Yamamoto et al. teach at least some of the integrated circuit switching elements arranged in cascaded fashion in order to reduce signal insertion loss (Yamamoto et al. – column 10 lines 25-67, and column 11 lines 1-2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Yamamoto et al. into the teachings of Gerlach et al. for the purpose of allowing the chip size to be remarkably reduced in the chip and reducing the insertion loss during transmission of the circuit with the impedance matching of the antenna with the receiver to be more easily achieved.

Consider **claim 15, as applied to claim 14 above**, Gerlach et al. as modified by Yamamoto et al. further teach wherein there are at least three receiver ports, any one receiver port selectably switched to be connected to the antenna port through at least two cascaded stages of integrated circuit switching elements (Gerlach et al. – column 2 lines 20-32, and column 2 lines 41-54; Yamamoto et al. – column 10 lines 25-67, and column 11 lines 1-2).

Consider **claim 16, as applied to claim 14 above**, Gerlach et al. as modified by Yamamoto et al. further teach wherein the integrated circuit switching elements are field effect transistors (Gerlach et al. – column 1 lines 51-62, and column 3 lines 37-63; Yamamoto et al. – column 5 lines 57-67, and column 6 lines 1-22).

Consider **claim 17**, Gerlach et al. teach a method of switching one of a plurality of transmitters and a plurality of receivers to a transmitter/receiver antenna (Abstract, column 1 lines 63-67, column 2 lines 4-6, column 2 lines 20-40, and column 3 lines 27-36), comprising the steps of:

connecting each transmitter to a respective one of a plurality of transmitter ports formed on a single integrated circuit die (column 1 lines 41-47, column 1 lines 63-67, column 2 lines 4-6, column 2 lines 20-32, column 2 lines 41-54, and column 3 lines 18-26);

connecting each receiver to a respective one of a plurality of receiver ports formed on the die (column 1 lines 41-47, column 1 lines 63-67, column 2 lines 4-6, column 2 lines 20-32, column 2 lines 41-54, and column 3 lines 18-26);

a plurality of switching topologies each associated with a respective one of the transmitter and receiver ports to connect a respective selected one of the transmitter and receiver ports to an antenna port formed on the die (column 1 lines 41-47, column 1 lines 63-67, column 2 lines 4-6, column 2 lines 20-32, column 2 lines 41-54, and column 3 lines 18-26).

However, Gerlach et al. fail to teach controlling a selected one of a plurality of switching topologies each associated with a respective one of the transmitter and receiver ports to connect a respective selected one of the transmitter and receiver ports to an antenna port formed on the die; and controlling other ones of the switching topologies to isolate others of the transmitter and receiver ports from the antenna port.

In the related art, Yamamoto et al. teach controlling a selected one of a plurality of switching topologies each associated with a respective one of the transmitter and receiver ports to connect a respective selected one of the transmitter and receiver ports to an antenna port formed on the die; and controlling other ones of the switching topologies to isolate others of the transmitter and receiver ports from the antenna port (column 5 lines 13-22, column 5 lines 57-67, column 6 lines 1-26, and column 6 lines 44-64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Yamamoto et al. into the teachings of Gerlach et al. for the purpose of allowing the chip size to be remarkably reduced in the chip and reducing the insertion loss during transmission of the circuit with the impedance matching of the antenna with the receiver to be more easily achieved.

Consider **claim 18, as applied to claim 17 above**, Gerlach et al. as modified by Yamamoto et al. further teach further including the steps of: arranging at least some of the switching topologies in cascaded stages including a first stage coupled to the antenna port and a last stage coupled to a plurality of the transmitter or receiver ports; connecting a selected one of the last said transmitter or receiver ports to the antenna ports by switching on the first stage, and switching on a switch associated with said selected one of the last said transmitter or receiver ports wherein the last said switch is a portion of the last stage; and switching off the remaining switching topologies and other switches in the last stage (Yamamoto et al. – column 8 lines 36-52, column 10 lines 2-24, column 10 lines 25-50, and column 12 lines 33-67).

Consider **claim 19, as applied to claim 18 above**, Gerlach et al. as modified by Yamamoto et al. further teach wherein said step of controlling a selected one of the switching topologies includes the step of switching a plurality of series-connected switching transistors to an ON state (Gerlach et al. – column 3 lines 18-63).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure (see PTO-892 Notice of References Cited).

Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the examiner should be directed to April S. Guzman whose telephone number is 571-270-1101. The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on 571-272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April S. Guzman
A.S.G/asg
05/16/07

EDAN ORGAD
PRIMARY PATENT EXAMINER
5/21/07